IN THE SPECIFICATION

Please replace the abstract with the following replacement abstract:

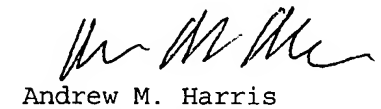
ABSTRACT OF THE DISCLOSURE

METHOD AND SYSTEM FOR ANALYZING QUIESCENT POWER PLANE CURRENT (IDDQ) TEST DATA IN VERY-LARGE SCALE INTEGRATED (VLSI) CIRCUITS

A method and system for analyzing quiescent power plane current test data in a very large scale integrated (VLSI) circuit provides diagnostic information and improved IDDQ testing for analyzing and detecting manufacturing defects in a VLSI device. A set of IDDQ test values is collected over a set of test vectors for a group of devices. The collected data is pared to remove values corresponding to defects, is correlated and pared again to remove stray values. A regression is generated for each vector from and IDDQ values for each vector and the IDDQ values at a selected reference vector. The IDDQ values at are normalized to an expected device/vector IDDQ value and cross-correlated to determine if the set is defect-free. New defect values are discarded and previously discarded values are potentially reclaimed. The above procedure is repeated until the set of non-defect vectors is stable and the IDDQ measurements categorized.

No additional fees should be incurred by this Amendment. However, If there are any fees incurred by this Amendment Letter, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully submitted,



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